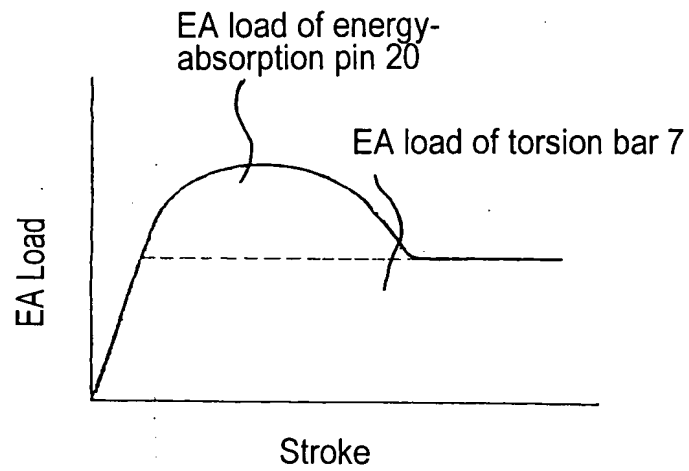


**Fig. 1**

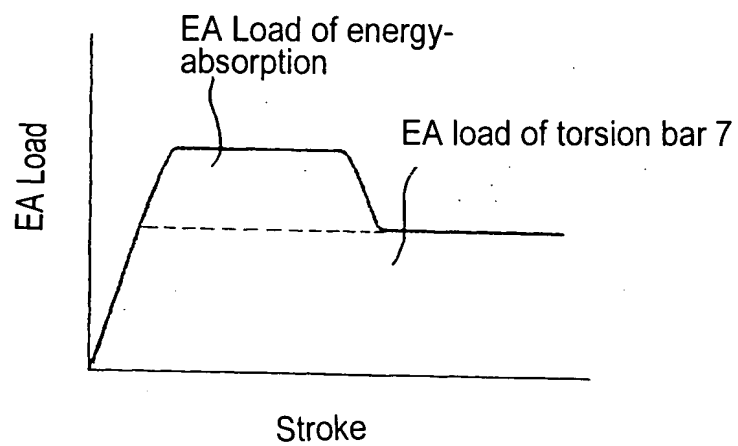
This diagram shows a cross-sectional view of a second embodiment of the device. It features a base layer 14a with a top surface 14b. A layer 14c is positioned on top of the base layer 14a. A layer 15 is located on top of layer 14c. A layer 20 is positioned between layer 15 and layer 14c. A layer 15a is located on top of layer 15. A layer 14 is located on top of layer 14c.

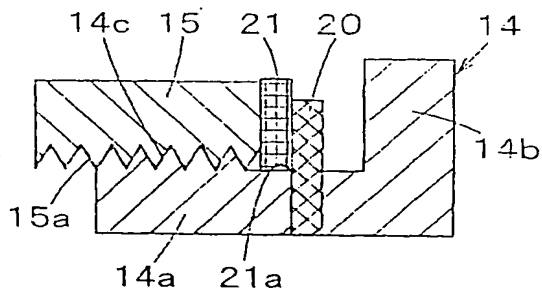
This diagram shows a cross-sectional view of a second embodiment of the semiconductor device. It features a substrate 14 with a top surface 14a. A first conductive layer 15 is formed on the top surface 14a, with a top surface 15a. A second conductive layer 14c is formed on the top surface 15a, with a top surface 14b. A third conductive layer 20 is formed on the top surface 14c, with a top surface 20a. The third conductive layer 20 is formed in a patterned manner, with a top surface 20b. The third conductive layer 20 is formed in a patterned manner, with a top surface 20b.

**Fig. 3(a)**

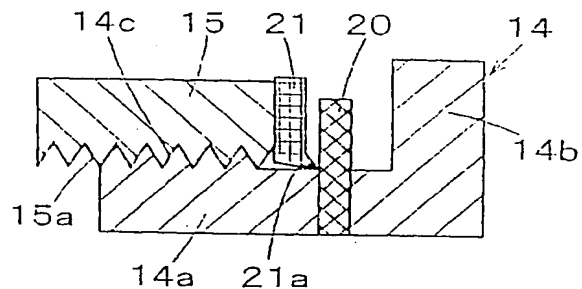


**Fig. 3(b)**

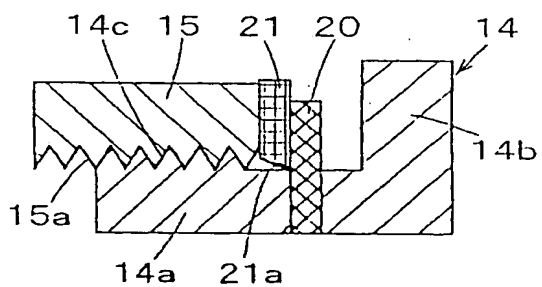




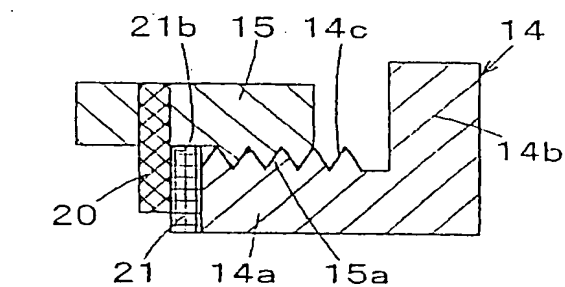
**Fig. 4(a)**



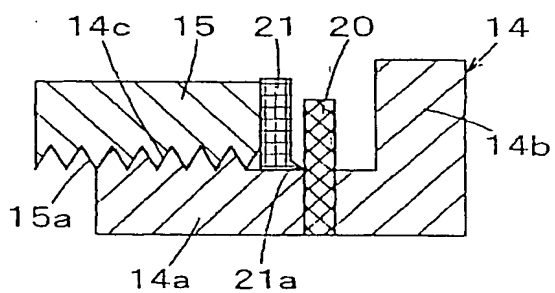
**Fig. 4(d)**



**Fig. 4(b)**



**Fig. 4(e)**



**Fig. 4(c)**

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**Fig. 5 Prior Art**

